Leo Marek

Lafayette, CA 94549 — Houston, TX 77005
+1 (925) 788 6276 | lnm7@rice.edu | leo.rice.edu | github.com/leomarek | linkedin.com/in/leo-marek

EDUCATION

Rice University | Houston, TX | *Masters in Electrical and Computer Engineering (ECE)* Dec 2026
Rice University | Houston, TX | *BS Electrical and Computer Engineering, BA Computer Science* **3.85 / 4.0** May 2026

- **Rice Engineering Alumni Leadership Excellence Award:** One of ten selected undergraduates from a pool of over 1,600.
- **Rice Sailing (Captain):** Compete at the highest level of college sailing - practice, classroom training, and 10+ weekends of competition travel annually. Led team to multiple top 3 finishes in conference and Regional Teams National Championship.
- **IEEE Vice President:** Plan IEEE socials, conferences, and recruiting events from top companies for 150+ ECE students.
- **Eta Kappa Nu:** Nominated and selected to honor society for being in top 1/4 of ECE class.
- **Teaching Assistant:** Instructed Python, data structures and algorithms, and signal processing to 400+ students across 3 courses.

Courses: Advanced VLSI Design, Advanced Computer Architecture, Digital Logic, Operating Systems, Compiler Construction, Algorithmic Thinking (Data Structures and Algorithms), Machine Learning, Parallel Programming, Signals and Systems, Random Signals

EXPERIENCE

ASIC Infrastructure Engineering Intern, *NVIDIA* | Santa Clara, CA May 2025 - Aug 2025

- Incoming - Will develop and optimize RTL and verification infrastructure to enhance GPU front-end build flow performance, contributing to scalable continuous integration systems and deploy solutions like containerization and distributed compute/storage.

Real Time DSP Computer Architecture Researcher, *RISC-V at Rice* | Houston, TX Aug 2024 - Present

- Engineering RISC-V very large instruction word architecture to accelerate preprocessing transforms for real time signal processing.
- Constructing custom benchmarks, ISA simulator, RISC-V VLIW compiler, and RTL processor implementation on FPGA.

Engineering Intern, *Team Engine* | Remote (California) May 2024 - Aug 2024

- Designed and built scalable features used daily by over 850 employers (impacting 200,000+ employees), including profile picture functionality and ML-powered survey insights, using TypeScript (React, Node), Python, ML APIs, and Docker.
- Collaborated with senior engineers on architecture decisions and delivered high-impact features critical to major sales, leveraging AWS, MySQL, and large language models.

Laboratory Assistant, *Oshman Engineering Design Kitchen* | Houston, TX Jul 2023 - Present

- Implemented software using AWS SQS and Lambda to interface with multiple APIs, save over 8 hours of manual data entry weekly, and manage makerspace tool access for over 1300 students.
- Instructed machine usage, assisted over 60 Design Project Teams working for clients from Hospitals to the Department of Defense.

SKILLS

Competencies	FPGA Development, Computer Architecture, Machine Learning, Embedded Systems, Scripting, Software Development, Low-Latency Systems, Real-Time Processing, Pipelining, Memory Hierarchy Optimization
Technologies	Verilog, HLS, Python, C/C++, Java, SQL, Typescript, HTML, CSS, Matlab, Git, Bash, LaTeX
Software	Vitis, Vivado, Simulink, Linux, AXI interface, Tensorflow, CUDA, VMware, Cloud, Docker, Kubernetes

SELECTED PROJECTS

FPGA-Accelerated Linear Algebra Engine for High-Throughput Compute Oct 2024 - Dec 2024

- Developed a hardware-accelerated linear system solver leveraging custom CORDIC, QR decomposition, back-substitution and matrix operations (matrix multiplication and matrix-vector multiplication) achieving 1500x speedup over ARM software implementation.
- Integrated for systolic processing with the AXI interface on Zynq-7000 SoC using Xilinx Vitis HLS, Vivado, and Model Composer.

Yalnix Operating System Jan 2024 - May 2024

- Developed a Unix-like OS with a kernel, file system, process scheduler, and virtual memory for RCS421 simulated hardware.
- Implemented process scheduling, context switching, and kernel/user mode protection for concurrent C program execution.
- Designed virtual memory with a two-level page table, TLB, and dynamic memory allocation, built a file system with demand paging, an LRU cache, and indirect inodes for large file storage, and developed system calls (Fork, Exec, Read/Write, etc.) alongside a terminal driver supporting multiple processes and virtual monitors.

FPGA Implementation of RISC Processor Oct 2023 - Dec 2023

- Executed in Verilog, simulated cycle-precise processor design using Icarus Verilog on central Linux cluster.
- Deployed on Spartan 7 FPGA using Xilinx Vivado, wrote custom assembly language programs for testing.

Low-Cost Negative Pressure Wound Therapy, Rice Bioengineering Jun 2023 - Jul 2023

- Assessed needs at five Costa Rican hospitals and led design of a low-cost, open-source negative pressure wound therapy device for low-resource settings.
- Built prototype with a team of four, developing embedded systems and custom UI on ESP32 in C++ despite limited tools and resources.